AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A ferroelectric liquid crystal display, comprising:

a liquid crystal display (LCD) panel including a plurality of gate lines, a plurality of data lines crossing the plurality of gate lines, and ferroelectric liquid crystal (FLC) material, wherein a plurality of liquid crystal cells arranged in a matrix pattern are defined by the crossings of the gate an data lines;

a plurality of thin film transistors connected to the gate and data lines, wherein each liquid crystal cell has a thin film transistor;

a gate driving circuit for applying substantially identical first and second scan pulses ~~at least twice~~ to each one of the plurality of gate lines during one frame period of the LCD panel; and

a data driving circuit for applying first and second data voltages having the same gray scale value ~~at least twice~~ to the data lines of the LCD panel in synchrony with the first and second scan pulses during the one frame period of the LCD panel,

wherein the first and second scan pulses are applied at an interval in time each other during the one frame period of the LCD panel; and

wherein the first and second data voltages are applied at an interval in time each other during the one frame period of the LCD panel.

2. (Original) The ferroelectric liquid crystal display according to claim 1, wherein the liquid crystal cell is a Half V-Switching Mode LFC cell.

3. (Original) The ferroelectric liquid crystal display according to claim 1, further comprising a timing controller for controlling the data driving circuit and the gate driving circuit.

4. (Currently Amended) The ferroelectric liquid crystal display according to claim 1, wherein the timing controller generates a multiple gate start pulse for causing the gate driving circuit to sequentially generate the first and second scan pulses ~~pulse~~ and for supplying the multiple gate start pulse to the gate driving circuit.

5. (Original) The ferroelectric liquid crystal display according to claim 1, wherein the multiple gate start pulse is generated at least twice during the one frame period of the LCD panel.

6. (Currently Amended) The ferroelectric liquid crystal display according to claim 1, wherein the data driving circuit applies identical first and second data voltages to the plurality of data lines ~~at least twice~~ during the one frame period of the LCD panel.

7. (Currently Amended) The ferroelectric liquid crystal display according to claim 6, wherein the data driving circuit maintains ~~a polarity~~ polarities of the first and second data voltages ~~voltage~~ applied to the data lines during the one frame period of the LCD panel.

8. (Currently Amended) The ferroelectric liquid crystal display according to claim 6, wherein the data driving circuit inverts ~~a polarity~~ polarities of the first and second data voltages ~~voltage~~ applied to the data lines at least once during the one frame period of the LCD panel.

9. (Currently Amended) The ferroelectric liquid crystal display according to claim 3, wherein the timing controller includes a memory device for storing data such that substantially identical first and second data voltages are suppliable to the LCD panel at least twice during the one frame period of the LCD panel.

10. (Currently Amended) A driving method of a ferroelectric liquid crystal display, comprising:

providing a liquid crystal display (LCD) panel including a plurality of gate lines, a plurality of data lines crossing the plurality of gate lines, and ferroelectric liquid crystal (FLC) material, wherein a plurality of liquid crystal cells arranged in a matrix pattern are defined by the crossings of the gate an data lines;

applying ~~substantially identical~~ first and second scan pulses ~~pulse at least twice~~ to each of the plurality of gate lines during one frame period of the LCD panel; and

applying first and second data voltages having the same gray scale value ~~at least twice~~ to the plurality of data lines in synchrony with the first and second scan pulses during one frame period of the LCD panel,

wherein the first and second scan pulses are applied at an interval in time each other during the one frame period of the LCD panel; and

wherein the first and second data voltages are applied at an interval in time each other during the one frame period of the LCD panel.

11. (Original) The driving method of the ferroelectric liquid crystal display according to claim 10, wherein the liquid crystal cell is a Half V-Switching Mode FLC cell.

12. (Currently Amended) The driving method of the ferroelectric liquid crystal display according to claim 10, further comprising generating a multiple gate start pulse for controlling the first and second scan pulses, wherein the multiple gate start pulse is generated at least twice during the one frame period of the LCD panel.

13. (Currently Amended) The driving method of the ferroelectric liquid crystal display according to claim 10, wherein the first and second data voltages ~~voltage~~ applied to the LCD panel within the one frame period of the LCD panel is identically applied.

14. (Currently Amended) The driving method of the ferroelectric liquid crystal display according to claim 13, wherein ~~a polarity~~ polarities of the first and second data voltages ~~voltage~~ applied to the LCD panel during the one frame period of the LCD panel is maintained.

15. (Currently Amended) The driving method of the ferroelectric liquid crystal display according to claim 13, wherein ~~a polarity~~ polarities of the data voltage applied to the LCD panel during the one frame period of the LCD panel is inverted at least once.